US009207909B1

(12) **United States Patent**
Langhammer

(10) **Patent No.: US 9,207,909 B1**

(45) **Date of Patent: Dec. 8, 2015**

(54) **POLYNOMIAL CALCULATIONS OPTIMIZED FOR PROGRAMMABLE INTEGRATED CIRCUIT DEVICE STRUCTURES**

(71) Applicant: **Altera Corporation**, San Jose, CA (US)

(72) Inventor: **Martin Langhammer**, Salisbury (GB)

(73) Assignee: **Altera Corporation**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 267 days.

(21) Appl. No.: **13/790,106**

(22) Filed: **Mar. 8, 2013**

Related U.S. Application Data

(60) Provisional application No. 61/729,797, filed on Nov. 26, 2012.

(51) **Int. Cl.**
G06F 7/544 (2006.01)

(52) **U.S. Cl.**
CPC *G06F 7/5443* (2013.01)

(58) **Field of Classification Search**
CPC combination set(s) only.
See application file for complete search history.

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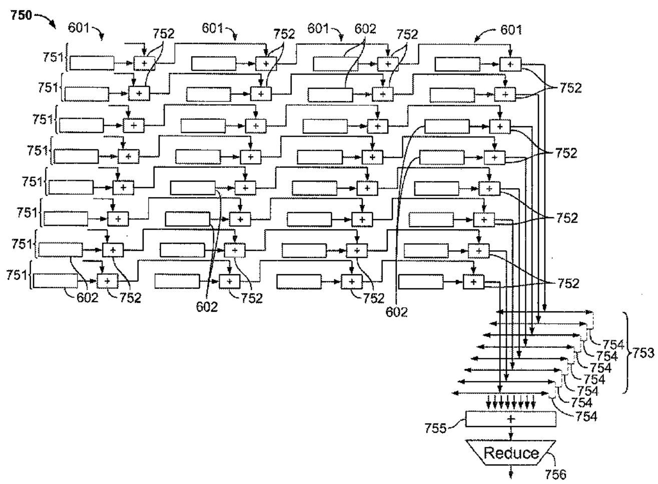
Primary Examiner — Chuong D Ngo
Assistant Examiner — Calvin M Brien
(74) *Attorney, Agent, or Firm* — Ropes & Gray LLP; Jeffrey H. Ingerman

(57) **ABSTRACT**

Polynomial circuitry includes a respective partial product generator for each bit position of each term of a plurality of terms of a polynomial to be evaluated. A respective plurality of adders for each bit position adds partial products of a respective bit position across all of the plurality of terms to provide a respective bit-slice sum. Resulting bit-slice sums are offset from one another according to their respective bit positions. A final adder adds together the respective offset bit-slice sums to provide a result.

18 Claims, 8 Drawing Sheets



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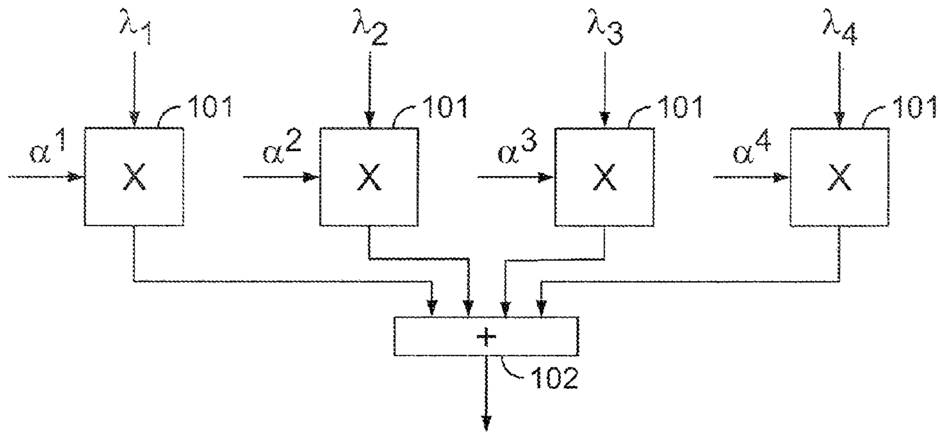

FIG. 1

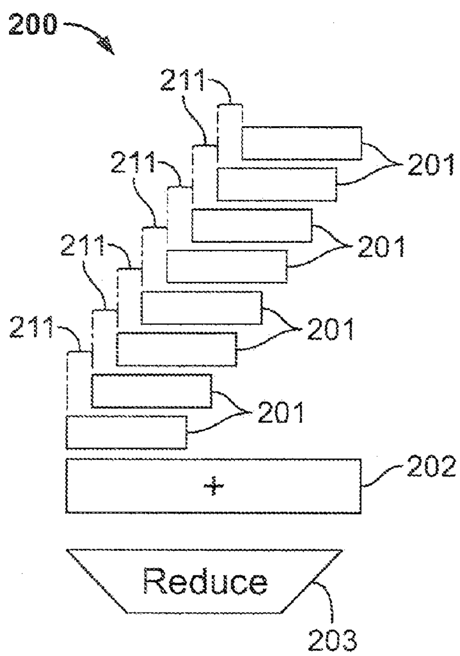

FIG. 2

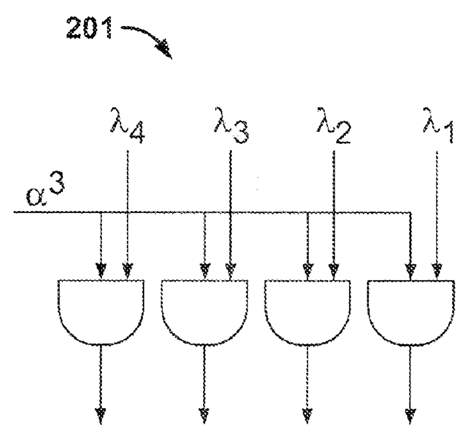

FIG. 3

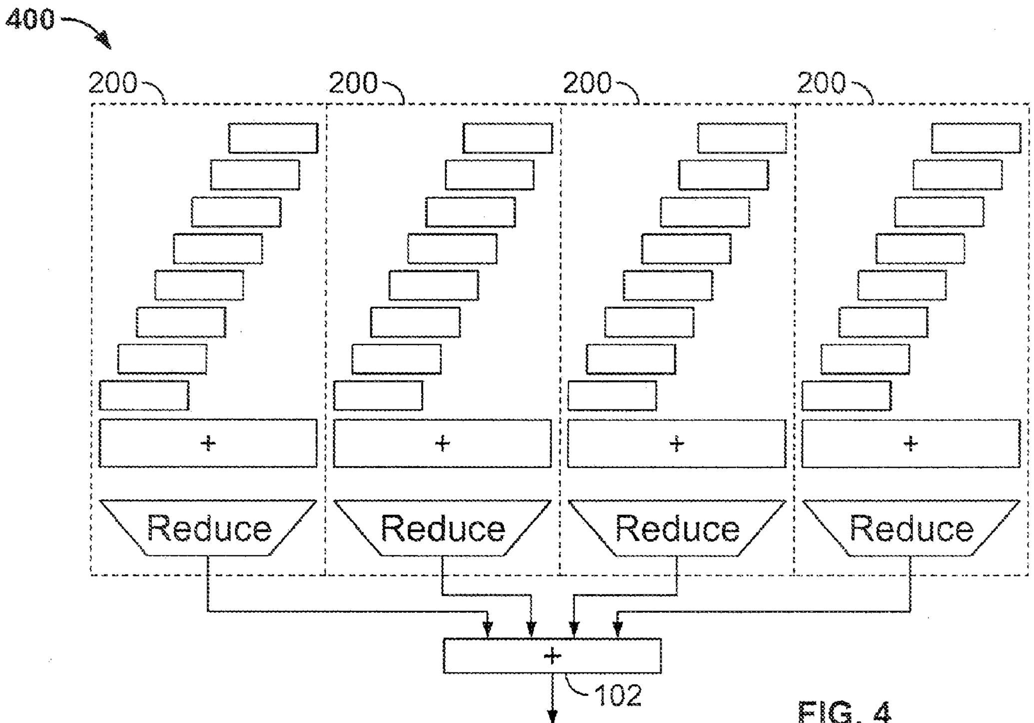
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FIG. 4

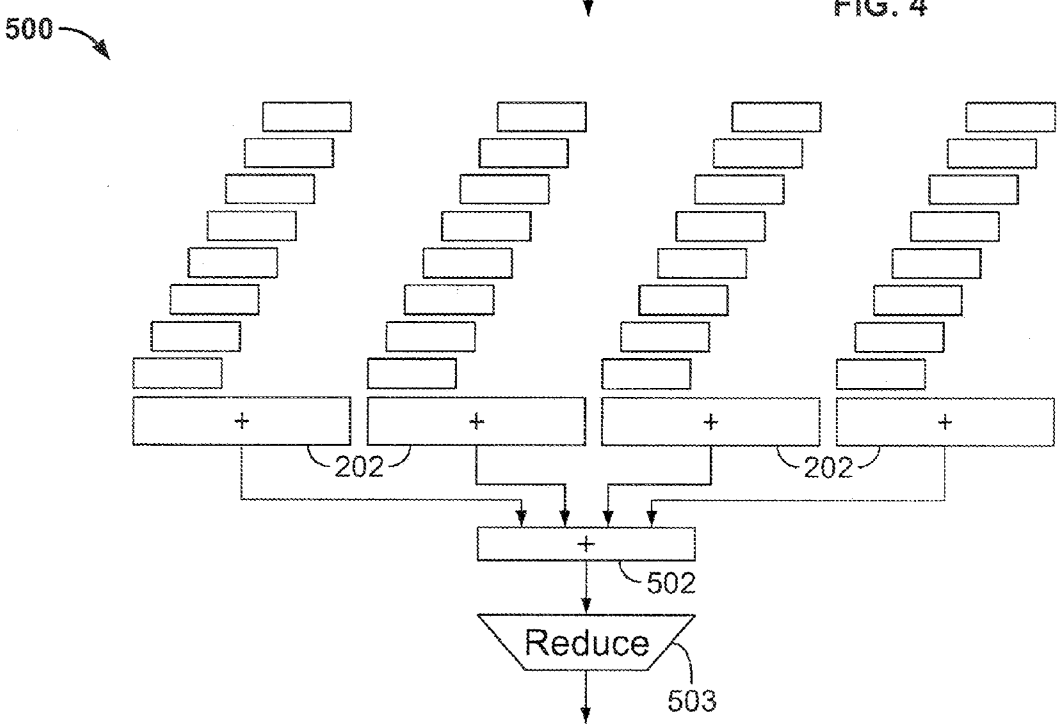
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FIG. 5

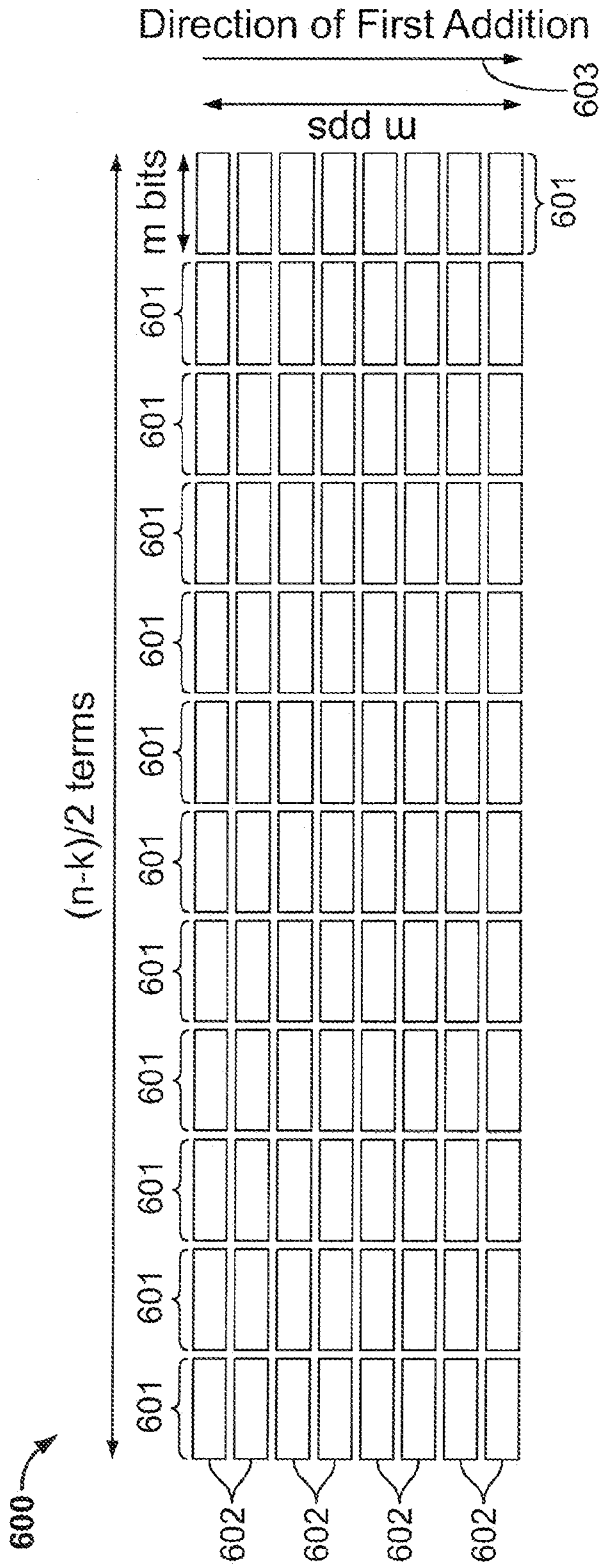
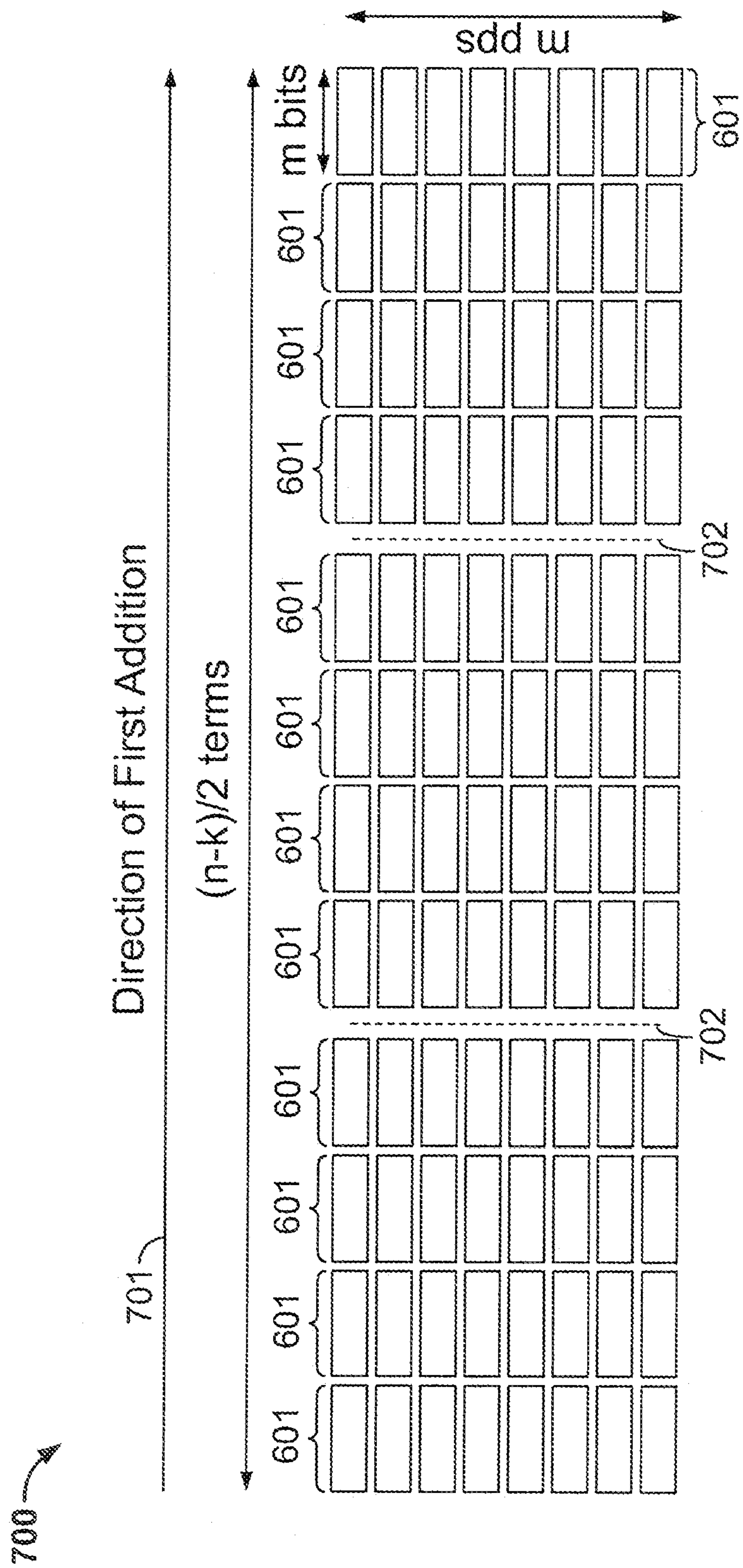


FIG. 6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(n-k)/2 terms
m bits
m pps
601
702

FIG. 7

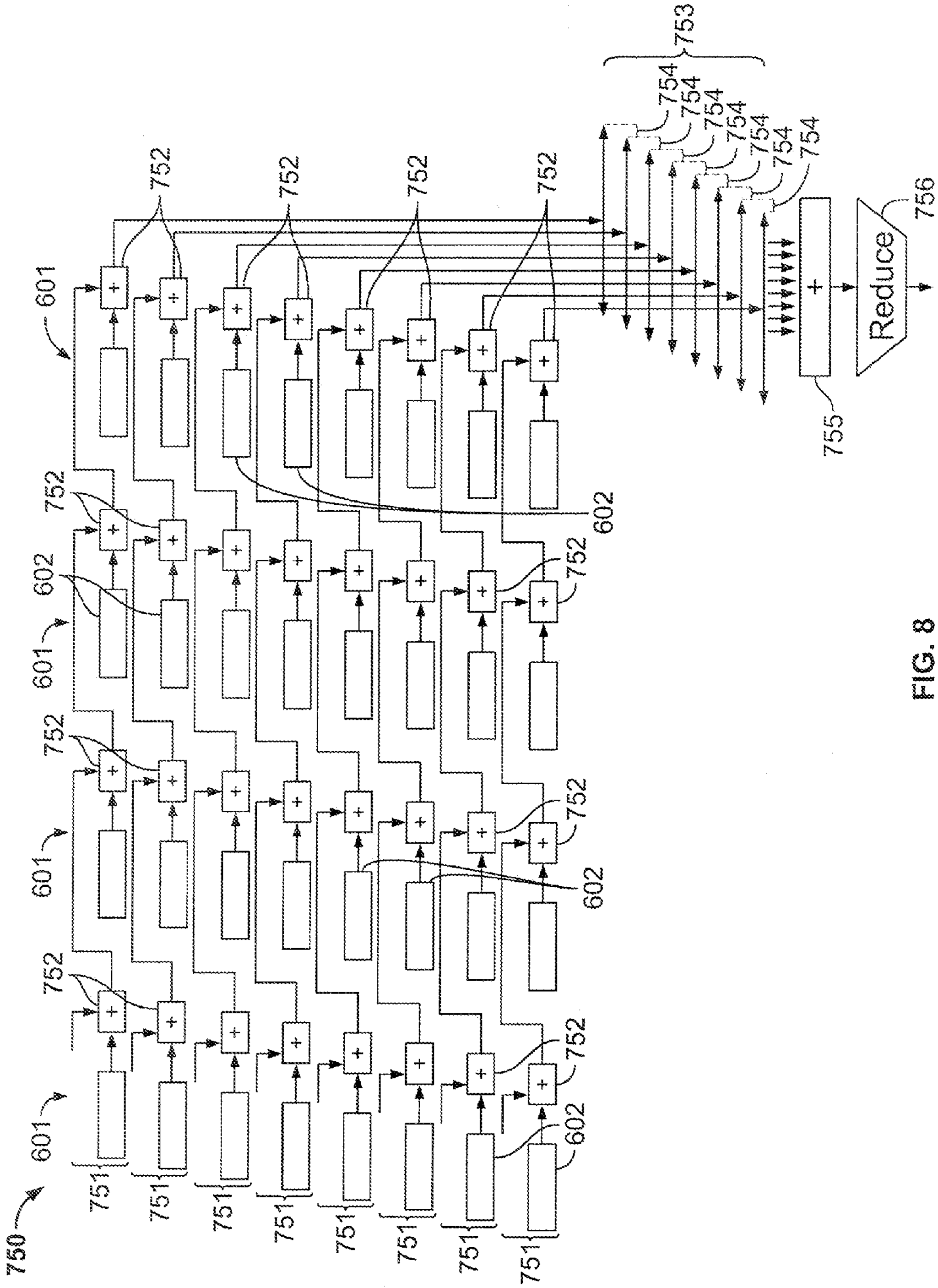


FIG. 8

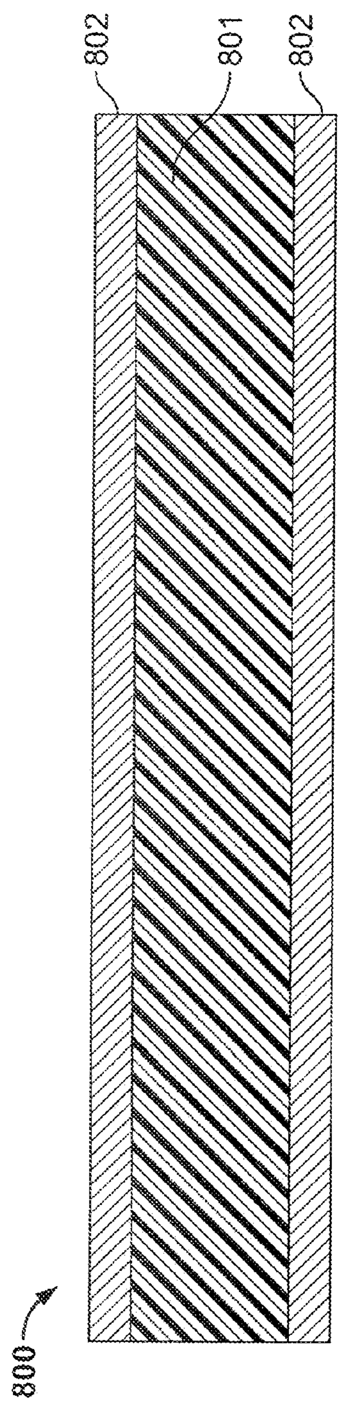


FIG. 9

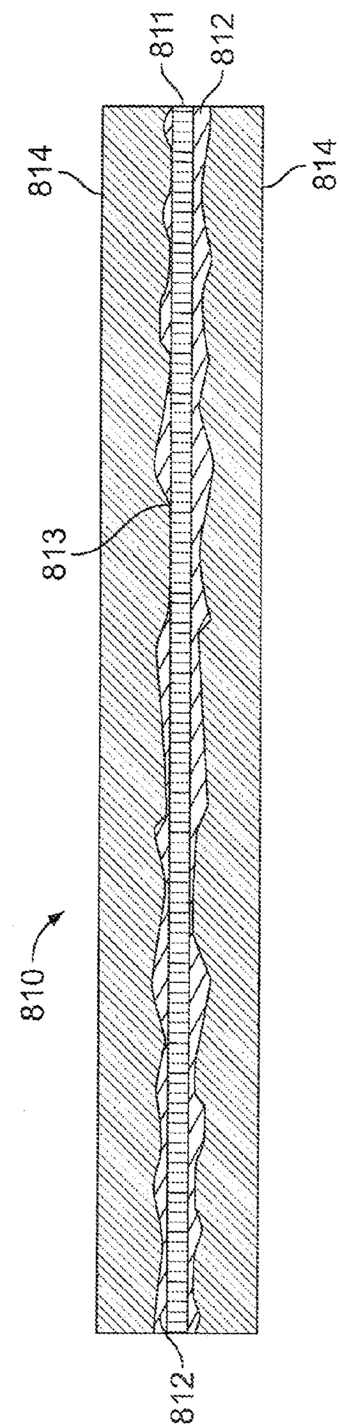
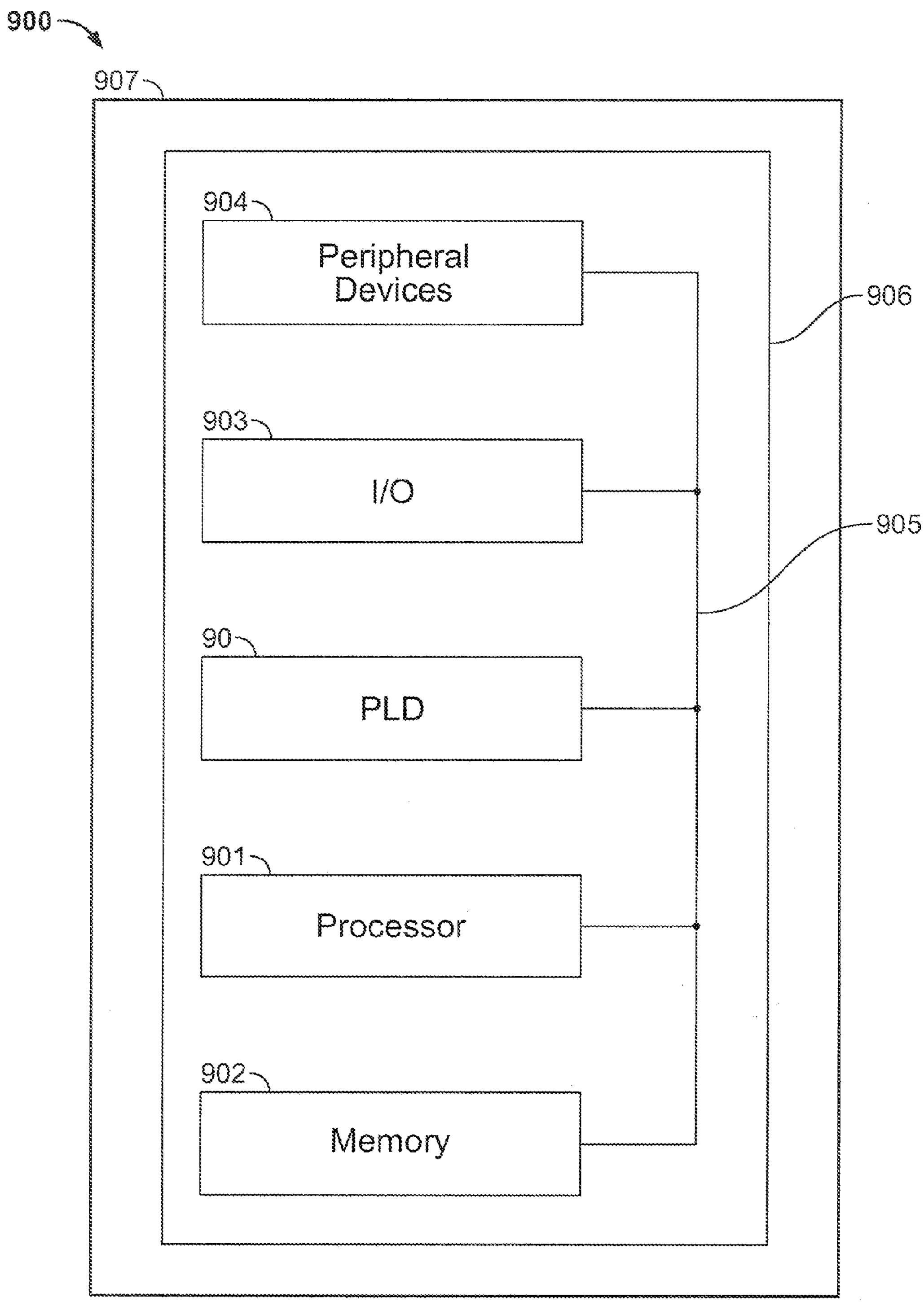


FIG. 10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PLD
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Processor
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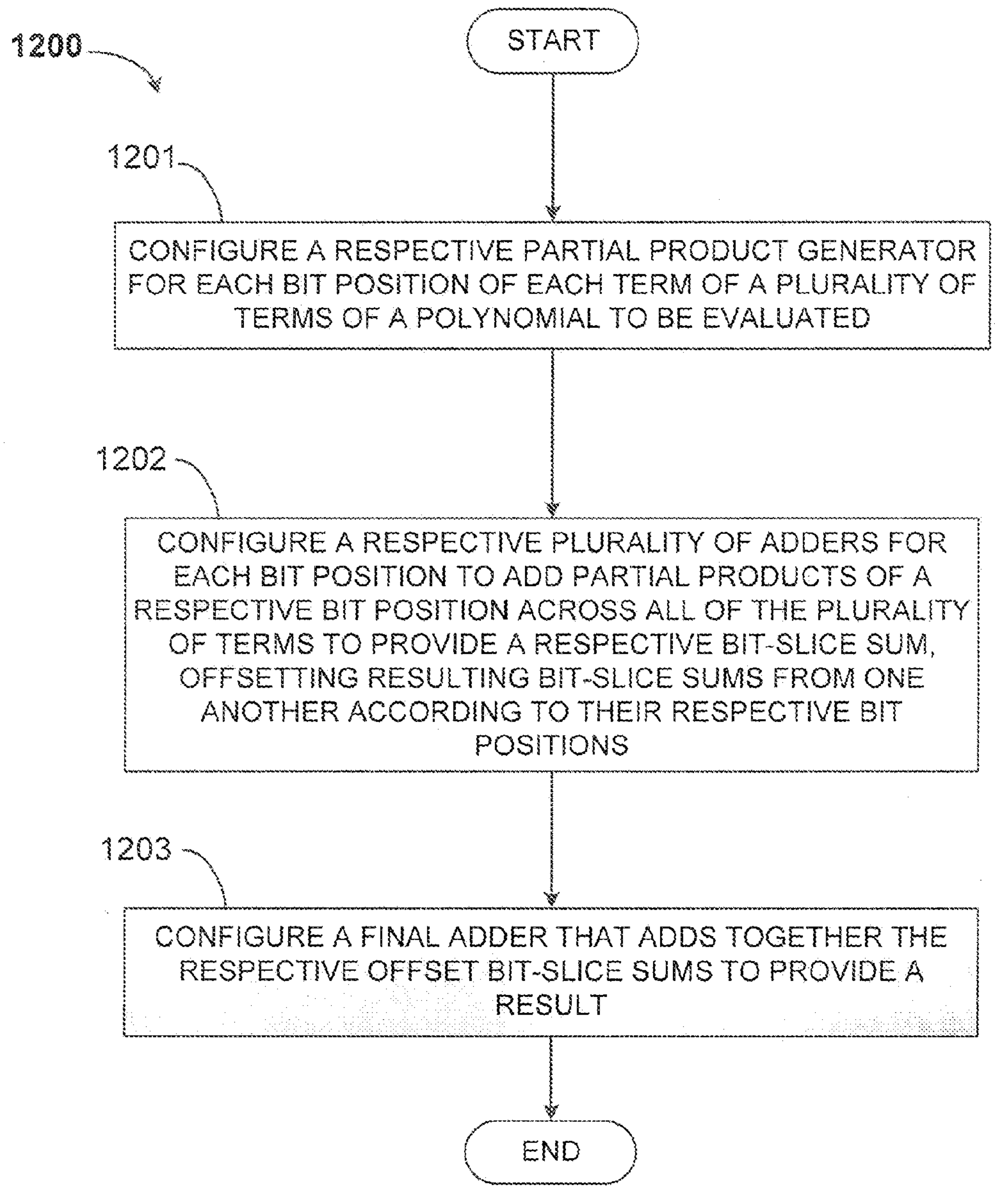
Memory

FIG. 11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START
1201
CONFIGURE A RESPECTIVE PARTIAL PRODUCT GENERATOR FOR EACH BIT POSITION OF EACH TERM OF A PLURALITY OF TERMS OF A POLYNOMIAL TO BE EVALUATED
1202
CONFIGURE A RESPECTIVE PLURALITY OF ADDERS FOR EACH BIT POSITION TO ADD PARTIAL PRODUCTS OF A RESPECTIVE BIT POSITION ACROSS ALL OF THE PLURALITY OF TERMS TO PROVIDE A RESPECTIVE BIT-SLICE SUM, OFFSETTING RESULTING BIT-SLICE SUMS FROM ONE ANOTHER ACCORDING TO THEIR RESPECTIVE BIT POSITIONS
1203
CONFIGURE A FINAL ADDER THAT ADDS TOGETHER THE RESPECTIVE OFFSET BIT-SLICE SUMS TO PROVIDE A RESULT
END

FIG. 12

POLYNOMIAL CALCULATIONS OPTIMIZED FOR PROGRAMMABLE INTEGRATED CIRCUIT DEVICE STRUCTURES

CROSS REFERENCE TO RELATED APPLICATION

This claims the benefit of commonly-assigned U.S. Provisional Patent Application No. 61/729,797, filed Nov. 26, 2012, which is hereby incorporated by reference herein in its entirety.

FIELD OF THE INVENTION

This invention relates to computing floating-point polynomials in programmable integrated circuit devices such as programmable logic devices (PLDs).

BACKGROUND OF THE INVENTION

Certain operations, such as certain memory operations, require evaluation of multiple shifted instances of the same polynomials. This is commonly done by adding multiple shifted partial products for each term, and then adding together all of those sums. However, such an operation may be inefficient when implemented in certain types of devices, particularly in programmable devices such as field-programmable gate arrays (FPGAs) that perform logic operations using arrangements of look-up tables (LUTs). In particular, because at or near both the most-significant bit and the least significant bit there are many empty positions, the addition operations do not pack efficiently into the LUTs.

SUMMARY OF THE INVENTION

The present invention relates to method and circuitry for implementing polynomial calculations using logic structures such as those found in programmable devices such as FPGAs. Instead of summing all of the partial products for each respective multiplier, and then adding together those sums, the partial products are summed across all multipliers in a bit-slice-by-bit-slice order. The sums of the bit slices are then in turn shifted by their relative indices and summed, and then reduced as necessary. Because the initial addition is across a bit slice, all bit positions within the sum will have similar hamming count—i.e., will be similarly populated. Therefore, the sums will pack efficiently into LUTs. Moreover, any level of pipelining can be used.

In accordance with embodiments of the invention, there is provided polynomial circuitry including a respective partial product generator for each bit position of each term of a plurality of terms of a polynomial to be evaluated. A respective plurality of adders for each bit position adds partial products of a respective bit position across all of the plurality of terms to provide a respective bit-slice sum. Resulting bit-slice sums are offset from one another according to their respective bit positions. A final adder adds together the respective offset bit-slice sums to provide a result.

A method of configuring a programmable device as such polynomial circuitry is also provided, and a non-transitory machine-readable data storage medium is provided that is encoded with software for performing the method of configuring such circuitry on a programmable device.

BRIEF DESCRIPTION OF THE DRAWINGS

Further features of the invention, its nature and various advantages will be apparent upon consideration of the following detailed description, taken in conjunction with the accompanying drawings, in which like reference characters refer to like parts throughout, and in which:

FIG. **1** shows a conceptual arrangement for evaluating shifted polynomials;

FIG. **2** shows schematically a circuit arrangement that can serve as one of the multipliers in FIG. **1**;

FIG. **3** shows schematically a circuit arrangement that can serve as one of the partial product generators in FIG. **2**;

FIG. **4** shows a circuit arrangement in which the arrangement of FIG. **2** is provided in place of each of the multipliers in FIG. **1**;

FIG. **5** shows an optimization of the arrangement of FIG. **3**;

FIG. **6** shows the order of operations in the arrangements of FIGS. **2-5**;

FIG. **7** shows the order of operations in accordance with embodiments of the present invention;

FIG. **8** shows a circuit arrangement in accordance with an embodiment of the present invention;

FIG. **9** is a cross-sectional view of a magnetic data storage medium encoded with a set of machine-executable instructions for performing a method according to the present invention;

FIG. **10** is a cross-sectional view of an optically readable data storage medium encoded with a set of machine executable instructions for performing a method according to the present invention;

FIG. **11** is a simplified block diagram of an illustrative system employing a programmable logic device incorporating the present invention; and

FIG. **12** is a flow diagram of an example of a method according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

One example of the use of embodiments of the current invention is the evaluation of Galois Field (or finite field) polynomials. When large Galois Field multiplier arrays (such as those used for a Chien search in Flash memory error-correcting codes, including BCH and Reed-Solomon codes) are used, the performance on an FPGA is greatly reduced because of the depth of logic. If the calculation is pipelined, the resource count increases significantly because of inefficiencies of packing the partial product calculations into LUTs effectively.

According to embodiments of the current invention, a Galois Field polynomial may be mapped in a new way onto FPGA logic structures. These embodiments can be used to quickly and efficiently evaluate polynomials for such applications such as the aforementioned Chien search used by BCH and Reed Solomon decoders. System performance requirements may require that these structures operate at speeds over 300 MHz, which may not be possible with previously known polynomial structures for FPGAs, particularly for some BCH applications that use larger field sizes (e.g., 13-15 bits).

A Chien search of polynomials requires one finite field multiplier for each polynomial term. If more than one location is checked at a time, the polynomial can be shifted to check another location by simply shifting each polynomial term. Shifting of the polynomial terms can be accomplished by multiplying each term with the required finite field value in multipliers **101**, and summing all of the multiplier outputs together in adder **102**, as shown in the arrangement in FIG. **1**, in which the an terms are Galois Field elements that represent powers of the roots of the field, and the Xn terms are Galois

Field elements that represent terms of the error locator polynomial (i.e., the polynomial being searched).

Each finite field multiplier **101** may have the structure **200** shown in FIG. **2**, in which there are m partial products **201** having m bits each, where m is the number of bits in the field. Each respective partial product may be generated by ANDing the λ_n input with a respective bit of the an input, as shown in the example of FIG. **3**, which shows example of a 4-bit polynomial term (λ) and one bit of a root powers value (α) generating one 4-bit partial product (in this case m=4). Each partial product is left shifted (**211**) by the bit position index of the bit in the second input to which it corresponds. The partial products are all summed in adder **202**, creating a value having 2m−1 bits. That number is then reduced back to m-bits at **203** using the irreducible polynomial for the field, according to any of various known reduction techniques.

Thus, the arrangement of FIG. **1** may have the structure **400** shown in FIG. **4**, with each multiplier **101** replaced with a copy of structure **200**. One way to improve the efficiency of structure **400** is to eliminate the individual reducers **203**, add the outputs of the various adders **202** in a further adder **502**, and then apply a single reduction **503**, as shown in FIG. **5**, and as described in copending, commonly-assigned U.S. patent application Ser. No. 12/719,770, which is hereby incorporated by reference herein in its entirety.

However, even with the structure of FIG. **5**, adding together all of the partial products still creates a potentially large number of values each having 2m−1 bits. This may create a very long logic path from the input finite field numbers α, λ to the output of the result. And if pipelining is used (by cutting the paths at any point, whether within or between the individual multipliers), the logic size may increase significantly, because of the uneven packing of the relatively shifted partial product bits into the LUTs, which increases as pipelining depth increases.

A solution in accordance with embodiments of the invention may be appreciated after considering FIGS. **6** and **7**.

FIG. **6** is a diagrammatic representation of the matrix **600** of operations performed by arrangements such as that of the circuit arrangement of FIG. **5**. Each multiplier is represented by a column **601**. There are (n−k)/2 multipliers, corresponding to the number of columns, where n is the number of bits (for BCH coding) or symbols (for Reed-Solomon coding) in the codeword, and k is the number of data bits or symbols in the codeword—i.e., (n−k) is the number of parity bits or symbols in the codeword. There are m partial product generators **602** per multiplier, each m bits wide. Relative shifts are not shown. As indicated by arrow **603**, the direction of first addition, corresponding to adders **202**, is downward.

It can be shown mathematically that the identical result would be obtained if, as in matrix **700** of FIG. **7**, the direction of first addition were horizontal as indicated by arrow **701**. This may be implemented, as one example, by the circuit arrangement **750** of FIG. **8**.

In arrangement **750**, each column **601** of partial products **602** still represents a single term of the polynomial being evaluated (the relative shifts are shown in this drawing). However, unlike in arrangement **500**, the partial products **602** in each of columns **601** are not added together in this case. Instead, the partial products **602** in each of rows **751** are added first. As shown here, this may be accomplished with a respective adder **752**. It will be appreciated that while the adders **752** are shown as being logically located in each respective row **751** between each respective column **601**, they may physically be present in those locations, but they also may be elsewhere on the programmable integrated circuit device and connected by routing resources of the programmable integrated circuit device to the respective partial product generators **602**.

After all of the rows **751** have been added, the resulting sums **753**, which are aligned with respective 1-bit offsets **754** as shown, are added by adder **755**, and then reduced at **756** from 2m−1 bits to m bits. Because the additions of rows **751** occur prior to the offsetting or shifting, they can be efficiently packed into the LUTs of a programmable device. Therefore, even if the addition operations are pipelined (possible cut points where pipelining may occur are shown at dashed lines **702** of FIG. **7**), there will be minimal additional programmable logic of the programmable device required to complete the additions. Although the final addition **755** occurs after offsetting or shifting, it is only one operation, so any inefficiency introduced at that point also has minimal effect.

As noted above, when arrangement **750** is constructed in programmable logic, adders **752** may be located elsewhere than between the partial product generators **602**. Indeed, both the partial product generators **602** and the adders **752** could be configured by a user completely from programmable logic resources along with programmable interconnect resources. As one alternative, separate dedicated multiplication circuits may be provided in hard-wired form on the programmable device and the user may use the programmable interconnect resources to create addition circuits and connect them to the dedicated multiplication circuits to form arrangement **750**.

One example of a method **1200** for configuring a programmable device as circuitry for evaluating a polynomial in accordance with an embodiment of the present invention is diagrammed in FIG. **12**. Method **1200** begins at **1201**, where, on the programmable device, a respective partial product generator is configured for each bit position of each term of a plurality of terms of a polynomial to be evaluated. Next, at **1202**, a respective plurality of adders is configured on the programmable device for each bit position, to add partial products of a respective bit position across all of the plurality of terms to provide a respective bit-slice sum, wherein resulting bit-slice sums are offset from one another according to their respective bit positions. Finally, at **1203**, a final adder that adds together said respective offset bit-slice sums to provide a result is configured on the programmable device.

Thus it is seen that circuitry and methods for efficiently performing polynomial calculations have been provided.

Instructions for carrying out a method according to this invention for programming a programmable device to perform polynomial calculations, may be encoded on a machine-readable medium, to be executed by a suitable computer or similar device to implement the method of the invention for programming or configuring PLDs or other programmable devices to perform operations as described above. For example, a personal computer may be equipped with an interface to which a PLD can be connected, and the personal computer can be used by a user to program the PLD using a suitable software tool, such as the QUARTUS® II software available from Altera Corporation, of San Jose, Calif.

FIG. **9** presents a cross section of a magnetic data storage medium **800** which can be encoded with a machine executable program that can be carried out by systems such as the aforementioned personal computer, or other computer or similar device. Medium **800** can be a floppy diskette or hard disk, or magnetic tape, having a suitable substrate **801**, which may be conventional, and a suitable coating **802**, which may be conventional, on one or both sides, containing magnetic domains (not visible) whose polarity or orientation can be altered magnetically. Except in the case where it is magnetic tape, medium **800** may also have an opening (not shown) for receiving the spindle of a disk drive or other data storage device.

The magnetic domains of coating **802** of medium **800** are polarized or oriented so as to encode, in manner which may be conventional, a machine-executable program, for execution by a programming system such as a personal computer or other computer or similar system, having a socket or peripheral attachment into which the PLD to be programmed may be inserted, to configure appropriate portions of the PLD, including its specialized processing blocks, if any, in accordance with the invention.

FIG. **10** shows a cross section of an optically-readable data storage medium **810** which also can be encoded with such a machine-executable program, which can be carried out by systems such as the aforementioned personal computer, or other computer or similar device. Medium **810** can be a conventional compact disk read-only memory (CD-ROM) or digital video disk read-only memory (DVD-ROM) or a rewriteable medium such as a CD-R, CD-RW, DVD-R, DVD-RW, DVD+R, DVD+RW, or DVD-RAM or a magneto-optical disk which is optically readable and magneto-optically rewriteable. Medium **810** preferably has a suitable substrate **811**, which may be conventional, and a suitable coating **812**, which may be conventional, usually on one or both sides of substrate **811**.

In the case of a CD-based or DVD-based medium, as is well known, coating **812** is reflective and is impressed with a plurality of pits **813**, arranged on one or more layers, to encode the machine-executable program. The arrangement of pits is read by reflecting laser light off the surface of coating **812**. A protective coating **814**, which preferably is substantially transparent, is provided on top of coating **812**.

In the case of magneto-optical disk, as is well known, coating **812** has no pits **813**, but has a plurality of magnetic domains whose polarity or orientation can be changed magnetically when heated above a certain temperature, as by a laser (not shown). The orientation of the domains can be read by measuring the polarization of laser light reflected from coating **812**. The arrangement of the domains encodes the program as described above.

A PLD **90** programmed according to the present invention may be used in many kinds of electronic devices. One possible use is in a data processing system **900** shown in FIG. **11**. Data processing system **900** may include one or more of the following components: a processor **901**; memory **902**; I/O circuitry **903**; and peripheral devices **904**. These components are coupled together by a system bus **905** and are populated on a circuit board **906** which is contained in an end-user system **907**.

System **900** can be used in a wide variety of applications, such as computer networking, data networking, instrumentation, video processing, digital signal processing, or any other application where the advantage of using programmable or reprogrammable logic is desirable. PLD **90** can be used to perform a variety of different logic functions. For example, PLD **90** can be configured as a processor or controller that works in cooperation with processor **901**. PLD **90** may also be used as an arbiter for arbitrating access to a shared resources in system **900**. In yet another example, PLD **90** can be configured as an interface between processor **901** and one of the other components in system **900**. It should be noted that system **900** is only exemplary, and that the true scope and spirit of the invention should be indicated by the following claims.

Various technologies can be used to implement PLDs **90** as described above and incorporating this invention.

It will be understood that the foregoing is only illustrative of the principles of the invention, and that various modifications can be made by those skilled in the art without departing from the scope and spirit of the invention. For example, the various elements of this invention can be provided on a PLD in any desired number and/or arrangement. One skilled in the art will appreciate that the present invention can be practiced by other than the described embodiments, which are presented for purposes of illustration and not of limitation, and the present invention is limited only by the claims that follow.

What is claimed is:

1. Polynomial circuitry for evaluating a polynomial having a plurality of terms, each term having a number of bit positions, said polynomial circuitry comprising:

a plurality of groups of partial product generators, each of said groups of partial product generators corresponding to a single term in said plurality of terms and, in each one of said groups of partial product generators, each respective partial product generator in said one of said groups of partial product generators providing an output value for a respective single input bit position of said single term to which said one of said groups of partial product generators corresponds;

adder circuitry for providing respective bit-slice sums, said adder circuitry comprising a plurality of respective groups of adders, each respective group of adders in said plurality of respective groups of adders including a number of adders equal in number to said plurality of terms and corresponding to one respective bit position in all of said plurality of terms, and summing output values of multiple ones of said partial product generators for said one respective bit position to provide said respective bit-slice sum having a respective bit-width, wherein resulting bit-slice sums are offset from one another, by less than their respective bit-widths, according to their respective bit positions, said plurality of groups of adders being equal in number to said number of bit positions; and

a final adder that adds together said respective offset bit-slice sums to provide a final result.

2. The polynomial circuitry of claim **1** wherein:

said terms have m bit positions; and

each respective partial product generator provides a partial result that is m bits wide.

3. The polynomial circuitry of claim **2** further comprising reduction circuitry that reduces width of said final result to m bits.

4. The polynomial circuitry of claim **1** further comprising reduction circuitry that reduces bit width of said final result.

5. The polynomial circuitry of claim **1** wherein each adder of said plurality of respective groups of adders is configured using at least one look-up table of a programmable integrated circuit device.

6. The polynomial circuitry of claim **5** wherein said programmable integrated circuit device comprises a field-programmable gate array.

7. A method of configuring a programmable device as circuitry for evaluating a polynomial having a plurality of terms, each term having a number of bit positions, said method comprising:

configuring, on said programmable device, a plurality of groups of partial product generators, each of said groups of partial product generators corresponding to a single term in said plurality of terms and, in each one of said groups of partial product generators, each respective partial product generator in said one of said groups of partial product generators providing an output value for a respective single input bit position of said single term to which said one of said groups of partial product generators corresponds;

configuring, on said programmable device, adder circuitry for providing respective bit-slice sums, said adder circuitry comprising a plurality of respective groups of adders, each respective group of adders in said plurality of respective groups of adders including a number of adders equal in number to said plurality of terms and corresponding to one respective bit position in all of said plurality of terms, and summing output values of multiple ones of said partial product generators for said one respective bit position to provide said respective bit-slice sum having a respective bit-width, wherein resulting bit-slice sums are offset from one another, by less than their respective bit-widths, according to their respective bit positions, said plurality of groups of adders being equal in number to said number of bit positions; and

configuring, on said programmable device, a final adder that adds together said respective offset bit-slice sums to provide a final result.

8. The method of claim **7** wherein:

said terms have m bit positions; and

said configuring a plurality of partial product generators comprises configuring each partial product generator to provide a partial result that is m bits wide.

9. The method of claim **8** further comprising configuring, on said programmable device, reduction circuitry that reduces width of said final result to m bits.

10. The method of claim **7** further comprising configuring, on said programmable device, reduction circuitry that reduces bit width of said final result.

11. The method of claim **7** wherein configuring adder circuitry comprises configuring each adder of said respective groups of adders using at least one look-up table of a programmable integrated circuit device.

12. The method of claim **11** wherein configuring adder circuitry comprises configuring each adder of said respective groups of adders using at least one look-up table of a field-programmable gate array.

13. A non-transitory machine-readable data storage medium encoded with non-transitory machine-executable instructions for configuring a programmable device as circuitry for evaluating a polynomial having a plurality of terms, each term having a number of bit positions, said instructions comprising:

instructions to configure, on said programmable device, a plurality of groups of partial product generators, each of said groups of partial product generators corresponding to a single term in said plurality of terms and, in each one of said groups of partial product generators, each respective partial product generator in said one of said groups of partial product generators providing an output value for a respective single input bit position of said single term to which said one of said groups of partial product generators corresponds;

instructions to configure, on said programmable device, adder circuitry for providing respective bit-slice sums, said adder circuitry comprising a plurality of respective groups of adders, each respective group of adders in said plurality of respective groups of adders including a number of adders equal in number to said plurality of terms and corresponding to one respective bit position in all of said plurality of terms, and summing output values of multiple ones of said partial product generators for said one respective bit position to provide said respective bit-slice sum having a respective bit-width, wherein resulting bit-slice sums are offset from one another, by less than their respective bit-widths, according to their respective bit positions, said plurality of groups of adders being equal in number to said number of bit positions; and

instructions to configure, on said programmable device, a final adder that adds together said respective offset bit-slice sums to provide a final result.

14. The non-transitory machine-readable data storage medium of claim **13** wherein:

said terms have m bit positions; and

said instructions to configure a plurality of partial product generators comprises configuring each partial product generator to provide a partial result that is m bits wide.

15. The non-transitory machine-readable data storage medium of claim **14** further comprising instructions to configure, on said programmable device, reduction circuitry that reduces width of said final result to m bits.

16. The non-transitory machine-readable data storage medium of claim **13** further comprising instructions to configure, on said programmable device, reduction circuitry that reduces bit width of said final result.

17. The non-transitory machine-readable data storage medium of claim **13** wherein said instructions to configure adder circuitry comprise instructions to configure each adder of said respective groups of adders using at least one look-up table of a programmable integrated circuit device.

18. The non-transitory machine-readable data storage medium of claim **17** wherein said instructions to configure adder circuitry comprise instructions to configure each adder of said respective groups of adders using at least one look-up table of a field-programmable gate array.

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